ORIGINAL ARTICLE

A Low-Power and Wide Dynamic Range Digital Pixel Sensor for Intrinsic Optical Imaging in Image-Guided Neurosurgery and Neocortical Epilepsy

Yasin Salehifar, Ahmad Ayatollahi *, Mohammad Azim Karami, Mahzad Pirghayesh Ghurshagh

School of Electrical Engineering, Iran University of Science and Technology, Tehran, Iran

*Corresponding Author: Ahmad Ayatollahi
Email: ayatollahi@iust.ac.ir

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Abstract

Purpose: Determining the borders of brain tumors, seizure foci, and their elimination in patients with brain tumors is very important in preventing cancer recurrence. Multispectral Optical Intrinsic Signal Imaging (MS-OISI) image-guided neurosurgery using visible-Near-Infrared (NIR) wavelengths have shown great potential for image-guided neurosurgery. One of the main challenges is the need for low-power consumption, high-speed and above 100dB dynamic range to capture both visible and NIR photons. The overarching goal of this work is to create a Digital Pixel Sensor (DPS) as a Complementary Metal-Oxide-Semiconductor (CMOS) camera for MS-OISI of the brain in image-guided neurosurgery that has a wide dynamic range, low power consumption, and high speed.

Materials and Methods: The general view of neurosurgical system, DPS, and circuit operation of conventional Pulsed Frequency Modulation (PFM) DPS are given first. The proposed PFM DPS and circuit implementation are shown, as well as simulation results obtained using a circuit simulator. Finally, a comparison with other similar works is given.

Results: The proposed pixel simulation results show that the performance parameters such as dynamic range and power consumption has improved in comparison to similar works. However, due to its complicated circuitry, it has a low spatial resolution, which can be compensated.

Conclusion: The image sensor is post-layout simulated in 0.18µm CMOS technology with a 1.3V supply voltage, resulting in 140dB dynamic range and 7.69µW power dissipation with a 11% fill factor. The key novelty for the proposed PFM DPS is: in-pixel Analog-to-Digital Conversion (ADC), using a low voltage and high-speed dynamic comparator. Furthermore, this work uses a self-reset mechanism, which eliminates the need for an external pulse source, as well as variable reference voltage, which eliminates the necessity for a global constant reference voltage. All of these features demonstrate the excellent potential of the proposed pixel for MS-OISI image-guided neurosurgery.

Keywords: Dynamic Range; Complementary Metal-Oxide-Semiconductor; Pulsed Frequency Modulation; Digital Pixel Sensor; Image-Guided Neurosurgery; Multispectral Optical Intrinsic Signal Imaging.

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1. Introduction

The invention of image-guided neurosurgery represents a significant advancement in the microsurgical treatment of tumors, seizure foci, and other intracranial lesions [1]. In many neurosurgery operations, image-guided neurosurgery plays a crucial role both as a preoperative and intraoperative aid to assess the area for surgical resection [2], since the procedure directly affects the patient's nerves or brain [3]. The complete removal of a tumor by neurosurgery is critical to the prognosis of patients with tumors, particularly those with brain tumors, the precision of tumor removal is crucial for preventing cancer recurrence and maintaining brain functionality [4]. Patients with refractory epilepsy may be able to go seizure-free after complete removal of epileptogenic brain areas where seizures originate [5]. During the preoperative assessment process for surgeries, a variety of screening technologies have been used [6-8], however, they only show the general position of brain tumors and seizure-inducing brain regions, missing their precise borders, in addition to being costly and bulky, they have poor spatial and temporal resolution [4,5,9]. Optical imaging tools have recently emerged as viable candidates for intraoperative diagnosis due to superior spatial resolution, real-time imaging capability, and low cost [4,10]. Optical Intrinsic Signal Imaging (OISI) is a form of biomedical optical instrument that can detect cortical activities by looking at the reflectance of specific wavelengths from the cortex, allowing OISI to assess physiological parameters like blood volume, hemoglobin concentration, and neuronal transitions [4,11-16]. Intraoperative intrinsic optical signal imaging has recently been found to be very useful in separating epileptic and tumorous cortices from eloquent brain areas [5,17], reducing surgical times for resecting cancerous tissue and seizure-inducing regions thus minimizing harm to healthy tissue [18].

Traditional OISI image acquisition techniques rely on scientific-grade Charge Coupled Devices (CCDs) [19, 20]. In this case, a good imaging performance is provided with a high quantum efficiency (number of generated charges to absorbed photons) and broadband sensitivity. CCD cameras, on the other hand, have a high read noise characteristic, requiring longer exposure times to achieve an acceptable Signal-to-Noise Ratio (SNR) to accurately detect minor signal variations. Upon imaging the live brain, long exposure intervals are a challenge because brain activity causes blurred images. CCD is also expensive, has a slow readout, consumes a lot of power, and is difficult to integrate with Complementary Metal-Oxide-Semiconductor (CMOS) complex circuits [21]. Due to a range of advantages over CCDs, CMOS image sensors (CISs), which can be divided into three categories: passive pixel sensor (PPS), active pixel sensor (APS), and Digital Pixel Sensor (DPS), have seen rapid growth. PPSs have simple pixels consisting of a photodiode and a single Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) switch, the circuit overhead cost is low and they have a high fill factor of 50 to 80 percent and, in turn, high spatial resolution for Multispectral Optical Intrinsic Signal Imaging (MS-OISI) image-guided neurosurgery. On the other hand, in spite of the small size capability and a large fill factor passive pixel sensors suffered from many limitations, such as high noise, slow readout, and difficult scalability which, in turn, low dynamic range, low speed for real-time imaging, low SNR and low sensitivity.

Customers' demand for miniaturized, low-power, and cost-effective imaging systems are driving this interest. Image sensors based on CMOS technology can incorporate a large amount of Very Large-Scale Integration (VLSI) electronics on-chip and hence the reduction of packaging costs. A single-chip camera with integrated timing and control electronics, sensor array, signal processing electronics, Analog-to-Digital Converter (ADC), and the complete digital interface is now easily envisioned [21-24].

The CISs are an excellent candidate for MS-OISI brain imaging due to their wide dynamic range, high sensitivity, high temporal and spatial resolution, low power consumption, and high speed (frame rate) [25, 26]. The minimum required dynamic range of CMOS image sensor for MS-OISI image-guided neurosurgery is above 100dB [25]. Several works have been documented to implement CMOS image sensors for OISI brain and image-guided neurosurgery, but they suffer from a low dynamic range, high power consumption, and low speed, and most of these works are focused on APSs [18, 27-33]. In addition, an n-MOS reset transistor and a source follower amplifier reduce the voltage swing by two transistor threshold voltages ($2V_{tn}$) [34]. As a result, the APS output voltage swing would be substantially limited as the technology scales, since the supply voltage reduction is faster than the threshold voltage reduction in technology evolution [34]. These factors result in a low dynamic range and a weak SNR [34]. On the other hand, time or frequency-mode CISs including DPSs have simple device architectures and higher SNR [35]. Each pixel in the DPS structure

undergoes digitization, which transforms the photodetector's analog output signal to a digital one. Among the most popular in-pixel ADC techniques are Pulse-Width Modulation (PWM) and Pulse-Frequency Modulation (PFM) [34]. The data restored with an analog signal is translated into time or frequency equivalents by these methods. The voltage domain's output constraints are bypassed in the time or frequency domain [34]. The DPS [34-38] has many advantages over analog sensors, including a broader dynamic range due to modulation techniques, which means the dynamic range is no longer limited by the power supply maximum [34], higher SNR, due to the proximity location of the ADC to point the signal is produced [34], improved scaling with CMOS technology due to reduced analog circuit output demands [34], lower Fixed-Pattern Noise (FPN) as a result of column FPN removal and column readout noise with CMOS technology.

A PFM DPS with an in-pixel variable reference voltage generator is proposed in this paper, with the appealing characteristics of wide dynamic range, low power consumption, high speed, and low voltage, making it suitable for use in MS-OISI brain imaging tools and surgery image-guided systems. This paper is structured as follows: section II depicts a conceptual diagram of an MS-OISI neurosurgical imaging system that can be used with the PFM DPS suggested in this paper as well as its operation. Section III discusses the proposed PFM DPS, its circuit implementation, and the key parameters of the designed sensor for MS-OISI image-guided neurosurgery, the simulation results and comparison with similar works in MS-OISI imaging are presented in section IV; and section V concludes this work.

2. Materials and Methods

2.1. MS-OISI Image-Guided Neurosurgery System Overview, Conventional PFM DPS, and Functionality

The conceptual block diagram of the OISI image-guided neurosurgery system for OISI imaging during tumor or epileptic focus resection and its components, including data acquisition board, data processing, the camera for monitoring surgical robot, haptics interface, and display panel for the surgeon are shown in Figure 1. The remainder of this paper focuses solely on the design and simulation of a single pixel to be arrayed in an imaging chip embedded in a CMOS camera for optical intrinsic signal imaging in neurosurgery (Figure 1. a. right).

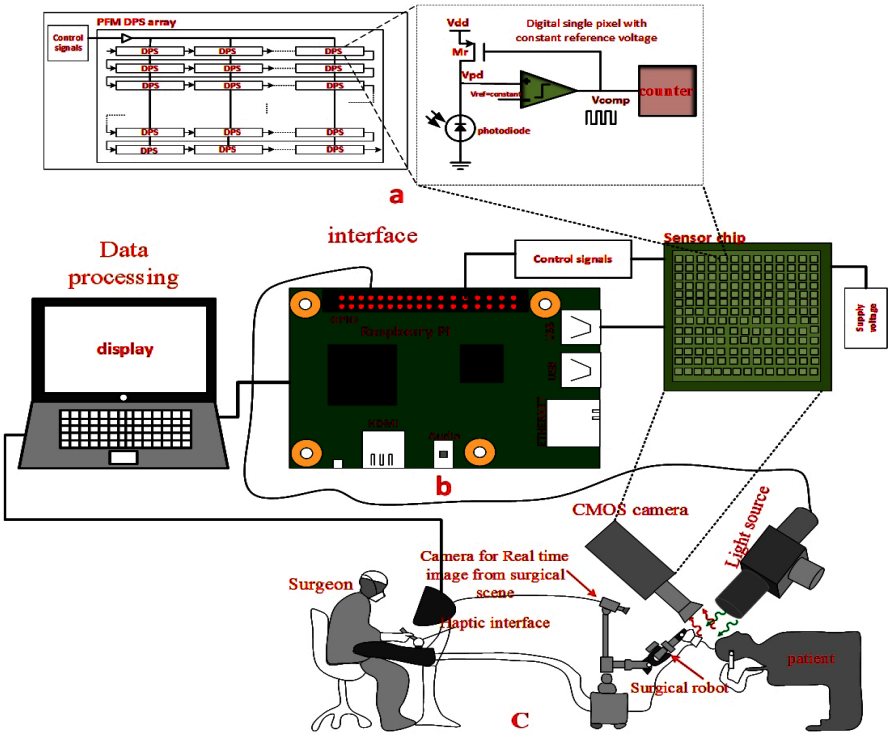

Figure 1. The conceptual representation of OISI image-guided neurosurgical imaging system setup: a) the PFM DPS chip block diagram (LEFT), the configuration of single PFM DPS pixel with a constant reference voltage (right). b) the platform is used for data acquisition as well as data processing from CMOS camera(left), sensor chip(right), c) telesurgical system for neurosurgical, and the CMOS camera is used for imaging as well as the light source

2.1.1. Conventional PFM DPS Pixel Operation

Figure 1. a (right) shows the schematic of a conventional PFM DPS with an in-pixel N-bit counter. A photodiode, open-loop comparator with a constant reference voltage, buffer, inverters, and a counter make the PFM DPS. The pixel captures images in two phases, namely the reset phase and the sensing phase. In the reset phase, the voltage across the Photodiode (PD) (V_{pd}) is charged to V_{dd} in the reset mode of operation, at this point, the reset transistor (M_r) is turned on and the comparator output (V_{comp}) is set to logic-1. The reset transistor is then turned off and begins the sensing mode. In the sensing phase, due to light absorption, the photodiode's conduction causes V_{pd} to decrease. The illumination level determines the photodiode current in I_{pd}. As V_{pd} reaches the constant reference voltage V_{ref}, the comparator output V_{comp} switches from logic-1 to logic-0, enabling the reset transistor (M_r) to turn on and charge the photodiode to V_{dd}. Since V_{pd}>V_{ref}, the comparator output is set to logic-1, turning off the M_r (P-channel Metal-Oxide Semiconductor (PMOS) transistor). The light intensity is represented by the in-pixel count, and this sensing process is repeated. However, using a conventional PFM DPS with a constant reference voltage across all pixel cells increases silicon cost and routing complexity, as well as lowering dynamic range, which is one of the most significant image sensor parameters for biomedical and image-guided neurosurgery.

PFM DPS output voltage pulse width can be determined using (Equation 1) [39]:

$$T_{pd} = \frac{(V_{dd} - V_{ref}) \times C_{pd}}{I_{pd} + I_d} \quad (1)$$

Where C_{pd} is the photodiode's total capacitance in the cathode, I_{pd} and I_d are the photodiode's current and dark current, and T_{pd} is the discharge period. In a single integration time, the number of pulses at the comparator output can be determined by (Equation 2) [39]:

$$N_{pixel} = \frac{T_{int}}{T_{pd}\dfrac{(I_{pd} + I_d) \times T_{int}}{(V_{dd} - V_{ref}) \times C_{pd}}} \quad (2)$$

2.2. The Proposed PFM DPS's Architecture and Circuit Implementation

This research develops a DPS structure based on pulse-frequency modulation. The proposed PFM DPS is depicted in Figure 2 as a block diagram. A photodiode, a Light-to-Frequency Converter (LFC) using a dynamic latch comparator with an in-pixel variable reference voltage, and a digital counter/shift register make up this circuit. The PFM DPS has a reference capacitor C_{ref} that generates reference voltage V_{ref} in conjunction with inverters. The proposed PFM digital pixel sensor's timing diagram is depicted in Figure 3, which is performed in parallel for all pixels and this leads to a high speed for real time imaging, the pixel captures images in two phases namely the reset phase and the sensing phase.

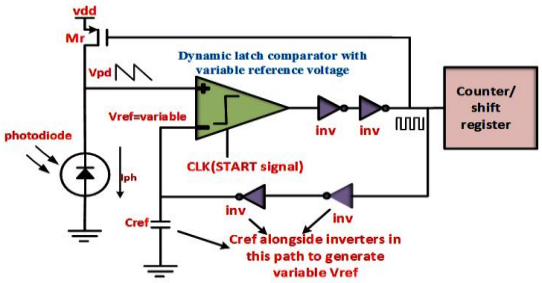

Figure 2. The proposed PFM digital pixel sensor architecture with an in-pixel reference voltage

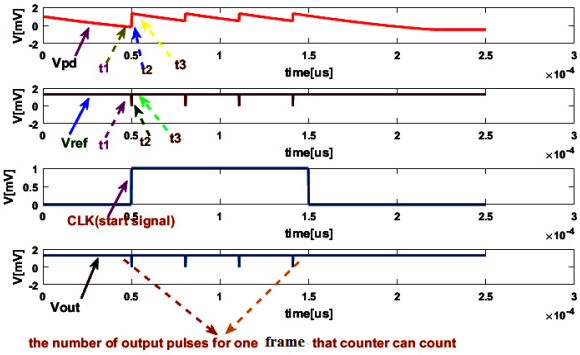

Figure 3. The timing diagram of the proposed DPS with an in pixel reference voltage for I_{ph}=14nA: a) photodiode voltage (V_{pd}) b) reference voltage (V_{ref}) c) comparator's output voltage (V_{out} or V_{comp})

In the reset phase, assuming that the comparator output is logic-0 at t1, CLK (START signal) is 0, the reset transistor M_r is on, and C_{pd} is charged to V_{dd} at t2. At t2, the inverters in the reference voltage path also reset C_{ref} and generate variable reference voltage V_{ref}. As a result, the comparator's output changes from logic-0 to logic-1. The reset transistor turns off at time t3, and begins the sensing mode. In the sensing phase, V_{pd} begins to fall at the rate determined by the illumination level. The reference capacitor C_{ref} is charged at the same time, and V_{ref} rises. The comparator's output changes to logic-0 when V_{pd} < V_{ref} is reached, and the cycle repeats.

The proposed PFM DPS's circuit schematic diagram is illustrated in Figure 4. A photodiode, a dynamic latch comparator, inverters and C_{ref}, in which the photodiode is a 15µm × 15µm n-well/p-sub diode. The dynamic latch comparator is made up of the optimized-preamplifier with an embedded regenerative latch, upon the signal Clk is low, and the comparator operation begins in a reset state. An N-type input pair (M_1, M_2) are the input stage. The outputs are pulled down during the reset state. The comparator chooses which input terminal has the highest voltage when Clk is high because M_4 , M_5, M_6, and M_7 are off and M_3 is on when Clk is high which is referred to as the regeneration state. The drain of its input transistor is driven down faster by the higher input voltage than the drain of the other input transistor. Upon the M_5 or M_6 turn-on voltage (threshold) is reached, the drain of the lower input voltage input transistor is pulled to V_{dd}. This ensures that the other M_5 or M_6 PMOS is turned off. The comparator latches on to this set of on/off devices. The input terminal with the greater voltage leads the matching output node to climb high at the end of the evaluation state. The inverters are used to restore signal levels.

In this approach, C_{ref} is used in conjunction with other inverters to generate variable V_{ref}. The channel width & length of the transistors are shown in Table 1. In the designed dynamic comparator, the input differential amplifiers are NMOS transistors for low supply voltage operation. This sort of comparator has the advantage of having no steady-state power consumption and high speed.

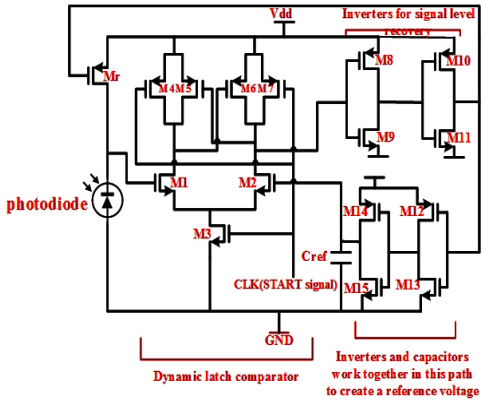

Figure 4. Circuit schematic of the proposed PFM DPS without counter

For the proposed pixel, a 10-bit Linear-Feedback Shift-Register (LFSR) counter with D flip-flops is also designed. Figure 5 depicts the counter's schematic representation. This type of shift register/counter has an advantage over the binary counter in that it has a relatively basic structure and a small number of parts. These advantages, together with the regular and compact layout, make it an excellent alternative for a digital image sensor. The issue with a linear feedback register is that it does not count as a binary sequence. As shown in Figure 5, SEL is the mode selection switching signal; if SEL = 0, the circuit functions as a counter; if SEL = 1, the circuit operates as a shift-register to serially output pixel information. The content of the shift-register, which sets the brightness level of the pixel, is a serial output from the pixel when signal EXTCLK is applied, and SERIALIN is the data input port used to reset the counter.

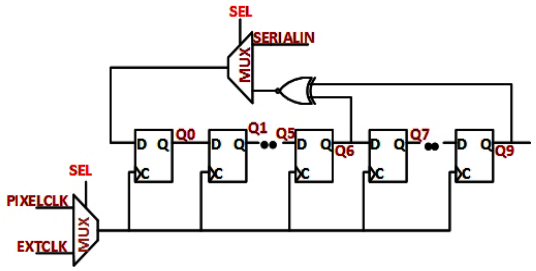

Figure 5. The 10-bit LFSR counter/shift register is depicted in schematic form

3. Results and Discussion

In 0.18µm CMOS technology, the suggested PFM DPS in the previous part is designed and post-layout simulated, and a comparison with similar works is given. Table 2 summarizes the simulation results of this study and compares them to recent studies. The proposed PFM DPS employs an n-well/p-sub photodiode, which is modeled as a current source coupled in parallel with the diode.

Table 1. Pixel transistor sizes

Transistor	W(µm)	L(µm)	Transistor	W(µm)	L(µm)
M1	1	0.18	M6	4	0.18
M2	0.5	0.18	M8,M9,M10,M11	1.5	0.18
M3	1	0.18	M12	1	0.18
M4,M7	2	0.18	13,M14,M15	0.5	0.18
M5	2.5	0.18	Mr	2.25	0.4

Table 2. A summary of the simulation results, as well as a comparison to prior similar studies

	[23]	[29]	[34]	[38]	[37]	[37]	**This work***
Technology (µm)	0.35	0.35	0.18	0.18	0.18	0.18	**0.18**
Pixel type	Self-reset	APS	PWM	PWM	Self-reset	Self-reset	**PFM**
Dynamic range (dB)	-	61	140	138	121	121	**140**
Fill factor (%)	29	26	21	-	4.4	4.4	**21**
Pixel size (µm×µm)	15×15	9.5×9.5	-	26×26	20×20	20×20	**30.34×36.57**
Power consumption (mW)	-	0.6(60 fps)	2.8nW(33fps)	-	-	-	$\mathbf{7.69\mu W}^{***}$
Transistors per pixel	11	-	-	-	-	-	**16***
Supply voltage(V)	3.6	3.3	0.8	1.8	3.3	3.3	**1.3**
Photodiode Structure	n-well/p-sub	n-well/p-sub	N+/p-sub	N-well/p-sub	Pinned photodiode	Pinned photodiode	**N-well/p-sub**

The most important parameters for the proposed PFM DPS, including DR, power consumption, frame rate and fill factor, which are among the most important parameters for MS-OISI image-guided surgery after simulation are extracted and reported. Most of these parameters for the proposed PFM DPS have been significantly improved compared to similar works. Although frame rate, which is important for real-time imaging has not been reported, the frame rate for the proposed PFM DPS in this paper is high due to the analog-to-digital converter at the pixel-level.

3.1. Power Dissipation

The power consumption of an image sensor is one of the most critical performance criteria for the imaging sensor in neuroimaging. A PFM DPS's total power dissipation is composed of both dynamic and static components that are affected by the illumination level and distribution (Equation 3, 4):

$$P_{tot} = P_{static} + P_{dynamic} \quad (3)$$

$$P_{static} = I_{CC} \times V_{CC} \quad (4)$$

For power analysis, PFM DPS's power usage is split into two components. Let P_1 denote the power consumed by the photodiode and reset transistor, and P_2 the power consumed by the comparator and feedback circuit. As a result, the power dissipation of the pixel is (Equation 5):

$$P_{pixel} = P_1 + P_2 \quad (5)$$

PFM DPS power dissipation analysis focuses mostly on dynamic power usage. The power consumption P_1 is mainly due to the charging up of C_{pd} by M_r and discharging of C_{pd} (Equation 6) [40].

$$P_1 = C_{pd}(V_{rst} - V_{ref})^2 f_{dis} \quad (6)$$

Where f_{dis} is the photodiode's charging/discharging cycle frequency. The power consumption P_2 is mainly composed of the comparator's and the feedback reset circuit's power consumption. The supply voltage V_{dd} determines the power consumption of the comparator P_{comp}. The energy used in a reset operation and the frequency of reset that PFM DPS utilizes self-reset determine the power consumption of the feedback circuit P_{rst}. Then P_2 is equal to [40]:

$$P_2 = (P_{comp} + P_{rst}) = (V_{dd}I + C_{load}V_{dd}^2 f_{dis}) \quad (7)$$

Adding P_1 and P_2 we obtain the total dynamic power [40]:

$$P_{pixel} = \left(C_{pd}(V_{rst} - V_{ref})^2 f_{dis} + V_{dd}I + C_{load}V_{dd}^2 f_{dis}\right) = \left(\left(C_{pd}(V_{rst} - V_{ref})^2 + C_{load}V_{dd}^2\right) f_{dis} + V_{dd}I\right) \quad (8)$$

For this purpose, the proposed PFM DPS in this paper has a supply voltage of 1.3V. The power consumption versus frame rate obtained from the proposed pixel is shown in Figure 6.

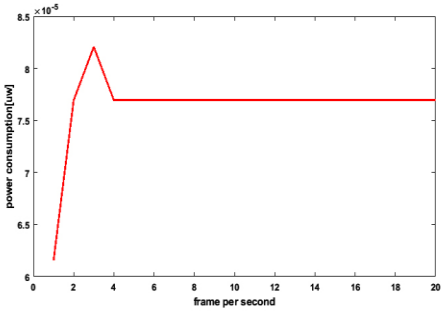

Figure 6. The power consumption versus frame rate(fps) for the proposed PFM DPS

The power dissipation for the proposed PFM DPS is 7.694μW, which is lower than similar works. Since a low voltage and a low power consumption comparator used in the designed pixel, which is dynamic, there is no steady-state power consumption that is the advantage of the dynamic comparator used in the designed pixel. The power consumption for the proposed PFM DPS is improved compared to most of the previous works ([18, 25, 27, 44-50]).

3.2. Dynamic Range

The dynamic range of an image sensor is another significant performance parameter. It is defined as the ratio of the greatest non-saturated signal strength to the minimum detectable signal strength. DR is defined as (Equation 9) [39]:

$$DR = 20\,log\frac{I_{max}}{I_{min}} \tag{9}$$

The proposed PFM DPS simulated for current between 10pA and 10μA are utilized to determine the relationship between the photodiode current and the pulse width of the comparator's output voltage (Figure 7).

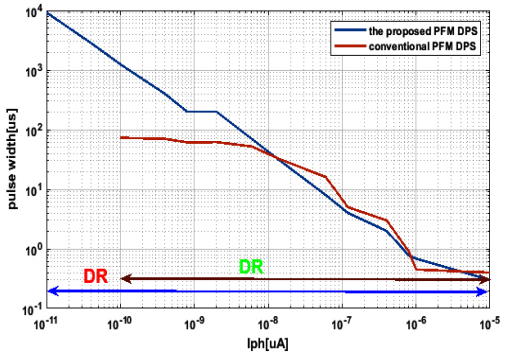

Figure 7. Dynamic range (photodiode current vs. comparator output voltage pulse width)

The proposed PFM DPS has a dynamic range of 140dB which means it can distinguish between different light intensities with improved resolution and image quality which is necessary to accurately determine the boundaries of tumors and other abnormalities in image-guided surgery. The dynamic range for the proposed PFM DPS is improved compared to the most similar works ([18, 25, 27, 44-50]).

The maximum detectable photodiode current is 10μA, and the pulse width has shrunk as sensitivity has increased, whereas the largest detectable photodiode current in a conventional PFM DPS with a constant reference voltage is just 700nA. In addition, the smallest photodiode current that can be detected is 1pA.

One of the shortcomings of the proposed PFM DPS is the long integration time which is needed for low illumination, which results in a greater pulse width of the comparator's output voltage and, as a result, reduced sensitivity. The suggested PFM DPS can be used in conjunction with an APD to improve sensitivity in low-illumination situations [41]. In addition, the output voltage for process corners simulations is depicted in the Figure 8.

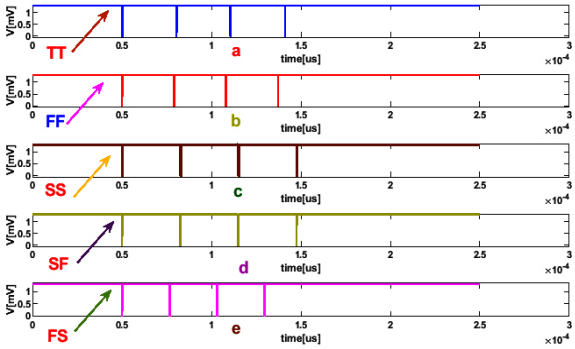

Figure 8. Output voltage for proposed PFM DPS in process corners for one image frame: a)TT b)FF c)SS d)SF e)FS

3.3. Fill Factor (FF)

The fill factor is another important performance parameter for MS-OISI image-guided surgery because the fill factor determines the spatial resolution for imaging. The Fill factor can be expressed simply as the ratio of the photodiode area (A_{pd}) to the entire pixel area (A_{pix}), is given by (Equation 10) [42]:

$$FF = \frac{A_{pd}}{A_{pix}} \times 100[\%] \tag{10}$$

Figure 9 depicts the proposed PFM digital pixel sensor's layout. The pixel size is 30.34μm × 36.57μm. The fill factor

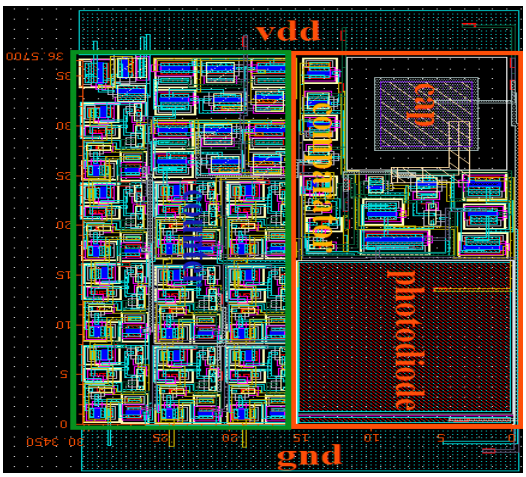

Figure 9. Proposed PFM digital pixel sensor layout

is around 21% (the ratio between the photosensitive area and the entire pixel surface is known as the fill factor). The pixel's poor fill factor (21%) is due to the pixel's complex pixel circuit, which Backside-Illuminated (BSI) technology can be used to compensate for the fill factor [43].

Table 2 demonstrates that the proposed PFM DPS has a larger DR than similar works ([29, 34-38]), which is owing to the usage of an ADC at the pixel level and a voltage-to-frequency conversion that is unaffected by variations in the supply voltage. Compared to reference [39], which uses an open-loop comparator, though dynamic range for reference [39] is higher and power consumption is lower, one of the disadvantages of reference [39] is long integration time in low-illumination which in turn reduces the pixel speed for real-time imaging in MS-OISI, but the proposed PFM DPS in this paper uses a dynamic comparator with control signal as a novelty for the proposed pixel which not only reduces static power but also increases speed, which is suitable for real-time MS-OISI imaging. One of the shortcomings of the designed pixel in reference [34], which is not reported in Table 2 is circuit conversion time, in the lower end of the light intensity is about 21 milliseconds (ms) which is not suitable for high speed and real time imaging in MS-OISI, however for the proposed PFM DPS in this paper conversion time in the lower end of the light intensity is 10 ms. Another disadvantage of reference [34] is the need for a global reset signal, which is required for all pixels, but the proposed PFM DPS in this paper is self-reset without the need for the global reset. Another shortcoming for reference [34] is the need for a global counter off-chip in addition to pixel-level static memory to read data, but the proposed pixel in this paper uses only one in-pixel counter/shift register, which is enough to read the data.

Also, the dynamic range of the proposed PFM DPS in this paper is higher than the new works ([18, 25, 27, 44-50]) offered for MS-OISI image-guided neurosurgery. Most of these works ([18, 25, 27, 44-50]) which some of them are based on APS and others are based on CCD focuses on improving the performance parameters of dynamic range, high speed for real-time imaging, SNR, power consumption and resolution. For most of these works ([18, 25, 27, 44-50]) the dynamic range obtained is below 120dB. The proposed PFM DPS in this paper also focuses on dynamic range, power consumption and high speed which can achieve high dynamic range (above 120dB), low power consumption and high speed because of the in-pixel ADC. Although this paper mainly focuses on the simulation of a single imaging pixel, the results of this paper are fully applicable to the CMOS camera for MS-OISI imaging during surgery in clinical and pre-clinical imaging applications which can be found in reference [25].

4. Conclusion

We presented a PFM DPS for CMOS camera in intrinsic optical imaging of the brain in image-guided Neurosurgery in this study to make a low-power, low voltage, low-area, and wide dynamic range image sensor. The designed pixel operation is verified using 0.18µm standard CMOS technology and post-layout simulation findings to validate the characteristics of the proposed circuit. The simulation findings reveal that it has a high dynamic range and low power consumption, indicating that it has a lot of potential for CMOS cameras in image-guided neurosurgery. The suggested PFM DPS has a 140 dB dynamic range and consumes 7.69µW power when powered by a 1.3V supply voltage. Compared to previous works, these parameters have been greatly improved. Low fill factor and longer pulse width of the comparator's output voltage in low light are two significant drawbacks of the proposed PFM DPS, the latter of which decreases the spatial resolution. BSI technology may compensate for the poor fill factor.

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